UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/577,399	05/22/2000	Jun Shi	INTL-0360-US (P8579)	4038

7590 04/04/2005

Timothy N Trop
Trop Pruner & Hu PC
Suite 100
8554 Katy Freeway
Houston, TX 77024

EXAMINER	
FAULK, DEVONA E	
ART UNIT	**PAPER NUMBER**
2644	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/577,399	SHI ET AL.	
	Examiner	Art Unit	
	Devona E. Faulk	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 17-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,17-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, filed 2/17/2005, with respect to the 112 rejection of claim 1 have been fully considered and are persuasive. The 112 rejection of claim 1 has been withdrawn.

2. Applicant's arguments,, filed 2/17/2005, with respect to the ~~21~~rejection(s)of claim(s) 5 under 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Kamiya and *In Re Harza 124 USPQ 378* (duplication of parts). The examiner has determined that the previous rejection (in first action mailed) using *In Re Harza* neglected to specifically point out to the applicant what feature was to be duplicated and further neglected to go into detail as to what In Re Harza entails. The applicant had argued previously, regarding In Re Harza that ~~that~~ duplication would involve using two codecs but the examiner should have made clear what would be duplicated. The examiner was referring to another pair of D/A converters and another mixer as the elements to be duplicated.

3. Claims 12-16 and 20-22 have been cancelled.

4. The applicant's request that the finality of the previous office actions be reconsidered has been granted. The applicant's argument was found to be persuasive and the examiner has withdrawn finality.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 1,4,5,6,8 and 11** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation (Audio Codec '97) in view of Kamiya (U.S. Patent 6,438,434) in further view of *In Re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960).

Regarding **claim** 1, Intel's document, Audio Codec '97, explaining the features, operation etc. comprises a block diagram of the functional blocks that make up the Audio Codec '97 (Figure 1)comprising a pair of D/A converters (DACs) which support a stereo PCM out channel which reads on " a first pair of digital to analog converters coupled to the first pair of stereo channels"; a digital interface ; a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer, which read on "a pair of analog to digital converters coupled to another one of said stereo channel pairs, one of said mixers also couple to said pair of analog to digital converters"; an analog mixer. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the

interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo channel pair. Intel fails to teach of a second pair of D/A converters coupled to another one of said stereo channel pairs, another mixer to output the other audio program and of a third stereo channel pair. However the concept of a multichannel codec having two mixers to receive two different channels was well known in the art as taught by Kamiya. Kamiya discloses a codec (Figure 1) having two stereo channel pairs, each coupled to a D/A converter (Figure 1 (1-3); Figure 4(93d,93e)) whose output is fed to a separate mixer (92b,92c; Figure 4). Kamiya further discloses in Figure 1 3 stereo channel pairs for a single codec (Figure 1). Furthermore it would have been obvious under duplication of parts, *In Re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing the second stereo channel separately. *In Re Harza* states that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced. The result of having a duplicate pair of D/A converters and another mixer to accommodate a second stereo channel pair would still yield the same result of converting a digital signal to an analog signal and providing that signal to a mixer.

Claim 4 claims the codec of claim 1 wherein said digital interface has a programmably changeable output data rate. Intel as

modified by Kamiya and Harza meets all elements of claim 1. Intel further discloses on page 14 and pages 61-62 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate.

Regarding **claim 5** Intel's document, Audio Codec '97, PCI accelerator, Figure 2); a codec coupled to processor (Figure 2); a block diagram of the functional blocks that make up the Audio Codec '97 (Figure 1) comprising a pair of D/A converters (DACs) which support a stereo PCM out channel which reads on " a first pair of digital to analog converters coupled to the first pair of stereo channels"; a digital interface ; a pair of A/D converters (ADCs) that supports two channels of fixed or variable rate input, the ADCs are coupled to the mixer, which read on "a pair of analog to digital converters coupled to another one of said stereo channel pairs, one of said mixers also couple to said pair of analog to digital converters"; an analog mixer. Intel does not teach specifically of a digital interface including a plurality of stereo channel pairs, but it does indicated that the interface can have extended functionality (Figure 10) with the addition of 4 PCM playback channels comprising the addition of PCM Center, L Surround, R Surround, LFE. Thus the digital interface certainly has the capability of processing more than 1 stereo channel pair. Intel fails to teach of a second pair of D/A converters coupled to another one of said stereo channel pairs, and another mixer to output the other audio program. However the concept

of a multichannel codec having two mixers to receive two different channels was well known in the art as taught by Kamiya. Kamiya discloses a codec (Figure 1) having two stereo channel pairs, each coupled to a D/A converter (Figure 1 (1-3); Figure 4(93d,93e)) whose output is fed to a separate mixer (92b,92c; Figure 4). Furthermore it would have been obvious under duplication of parts , *In Re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960), to incorporate the additional D/A converters and mixer for the benefit of processing the second stereo channel separately. *In Re Harza* states that the mere duplication of parts has no patentable significance unless a new and unexpected result is produced. The result of having a duplicate pair of D/A converters and another mixer to accommodate a second stereo channel pair would still yield the same result of converting a digital signal to an analog signal and providing that signal to a mixer.

All elements of **claim 6** are comprehended by the rejection of claim 5.

Claim 8 claims the processor-based system of claim 5 wherein said system can process two separate audio programs at the same time. Intel as modified by Kamiya and Harza meets all elements of that claim. As stated above apropos of claim 5, Kamiya teaches of processing two audio programs at the same time.

Claim 11 claims the codec of claim 5 wherein said digital interface has a programmably changeable output data rate. As stated above apropos of claim 1, Intel's Audio Codec '97 as modified by Kamiya and Harza meets all elements of that claim. Intel discloses

on page 14 and pages 61-62 that the AC 097 analog component can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate.

7. **Claims 2 and 9** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation (Audio Codec '97) in view of Kamiya (U.S. Patent 6,438,434) in further view of *In Re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960) in further view of Malcolm, Jr. et al. (U.S. Patent 6,301,366).

Claims 2 and 9 claim the codec of claim 1 and the processor-based system of claim 5 respectively further including a Sony/Phillips digital interconnect formatter (SPDIF). Intel as modified by Kamiya and Harza meets all elements of claims 1 and 5 but fails to disclose a SPDIF. Malcolm discloses a single chip audio system including a SPDIF (column 12, lines 40-45). A SPDIF allows the transfer of audio from one file to another without the conversion to and from an analog format, which could degrade signal quality. It would have been obvious to modify Intel as modified by Kamiya and Harza by further including a SPDIF as taught by Malcolm in order to allow for the transfer of audio without degrading the signal quality.

8. **Claims 3 and 10** are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation (Audio Codec '97) in view of Kamiya (U.S. Patent 6,438,434) in view of *In Re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960) in further view of Adams et al. (U.S. Patent 5,452,348).

Claims 3 and 10 claim the codec of claim 1 and the processor-based system of claim 5 wherein said digital interface includes a plurality of programmable ports so that the connections from the digital interface to said digital-to-analog converters might be changed. Intel as modified by Kamiya and Harza meets all elements of claims 1 and 5 but fails to disclose wherein said digital interface includes a plurality of programmable ports. However this concept was well known in the art at the time of filing as taught by Adams. Adams discloses a processor-based system that can programmably change the assignment of agent telephone units to different ports (column 7, lines 39-52). The applicant's recited claim language of "so that the connections from the digital interface to said digital-to-analog converters might by changed" is intended use. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Intel as modified by Kamiya and Harza by using Adams concept of programmably changing port assignments in order that assignments could be changed without damaging the physical location or switch I/O port.

9. **Claim 7 is** rejected under 35 U.S.C. 103(a) as being unpatentable over Intel Corporation (Audio Codec '97) in view of Kamiya (U.S. Patent 6,438,434) in further view of *In Re Harza*, 274 F. 2d 669, 124 USPQ 378 (CCPA 1960) in further view of Mayo (U.S. patent 5,133,081).

Claim 7 claims the processor-based system of claim 6 wherein said system may simultaneously play one audio program while recording another audio program. Intel as modified by Kamiya and Harza meets all

elements of that claim. Intel teaches of a machine-readable media (40) capable of storing recorded karaoke data. Mayo discloses a system comprising two codecs capable of simultaneously recording and playing messages using the same recording medium (column 10, lines 42-46). It would have been obvious to one of ordinary skill in the art at the time of the invention to use Mayo's concept of simultaneously recording and playing in order to allow simultaneous recording and playback.

10. **Claim 17** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (U.S. Patent 6,438,434) in view of Adams et al. (U.S. Patent 5,452,348).

Regarding **claim 17**, Kamiya discloses an article (computer) comprising a medium storing instructions (personal computer executes various signal processing such as D/A and A/D conversions; there is implicitly some medium that permits the computer to execute processing; column 5, lines 38-47) that enable a processor-based system to receive at least two digital audio programs (codec, Figure 1); convert each of said digital audio programs to an analog format (D/A converters, 1-3; Figure 1); output each of said audio programs to a different port (Figure 1). Kamiya fails to disclose programmably changing the assignment of said programs to said ports. However this concept was well known in the art at the time of filing as taught by Adams. Adams discloses a processor-based system that can programmably change the assignment of agent telephone units to different ports (column 7, lines 39-52). Therefore, it would have been obvious to one

of ordinary skill in the art at the time of the invention to modify Kamiya by using Adams concept of programmably changing port assignments in order that assignments could be changed without damaging the physical location or switch I/O port.

11. **Claim 18** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (U.S. Patent 6,438,434) in view of Adams et al. (U.S. Patent 5,452,348) in further view of Intel Corporation (Audio Codec '97).

Claim 18 claims the article of claim 17 further storing instructions that enable the processor- based system to programmably change the data rate of at least one of said audio programs. Kamiya as modified by Adams meets all elements of claim 17. Kamiya as modified by Adams fails to teach of programmably changing the data rate as claimed. Intel discloses an audio codec, on page 14 and pages 61-62, that can perform fixed or variable sample rated DAC and ADC conversions. Thus data output from the digital interface can have a programmed changeable output data rate. It would have been obvious to modify Kamiya as modified by Adams by programmably changing the data rate as taught by Intel for the benefit of being able to process different types of audio sources.

12. **Claim 19** is rejected under 35 U.S.C. 103(a) as being unpatentable over Kamiya (U.S. Patent 6,438,434) in view of Adams et al. (U.S. Patent 5,452,348) in further view of Mayo (U.S. patent 5,133,081).

Claim 19 claims the article of claim 17 further storing instructions that enable the processor-based system to play one audio

program while recording another audio program. Kamiya as modified by Adams meets all elements of claim 17. Kamiya as modified by Adams fails to disclose the processor-based system being able to play audio program while recording another. Mayo discloses a system comprising two codecs capable of simultaneously recording and playing messages using the same recording medium (column 10, lines 42-46). In the context of Kamiya teaching of multiple inputs for a single codec, it would have been obvious to one of ordinary skill in the art at the time of the invention to use Mayo's concept of simultaneously recording and playing in order to allow simultaneous recording and playback.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Devona E. Faulk whose telephone number is 571-272-7515. The examiner can normally be reached on 8 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on 571-272-7564. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DEF

SINH TRAN
SUPERVISORY PATENT EXAMINER